APPLICATION NOTE

TDA9952 CCD
SIGNAL PROCESSOR

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Philips
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APPLICATION NOTE

TDA9952 CCD SIGNAL PROCESSOR

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CONTENTS

1 INTRODUCTION

The TDA9952 is an analog to digital interface for CCD based cameras. This chip includes a correlated double sampling block (CDS), an optical black calibration loop, a programmable gain amplifier (PGA), a low power 10-bits analog to digital converter (ADC) and an 8-bits digital to analog converter (DAC) for additional system controls. The PGA, DAC, black reference and other control pulses polarities are programmed through a simple 3 wires serial interface.

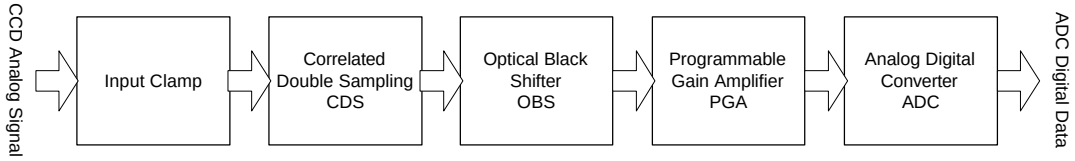

Figure 1. Philips CCD preprocessor features

2 CCD VIDEO SIGNAL

Light falling on CCD pixels generates charges, which are sensed with a capacitor. This sensing capacitor must be reset to a reference level thanks to a MOS switch before being filled with pixel's charges. The video signal is the voltage shift at the sensing capacitor.

The CCD output signal can be decomposed into three steps as described on Figure 2.

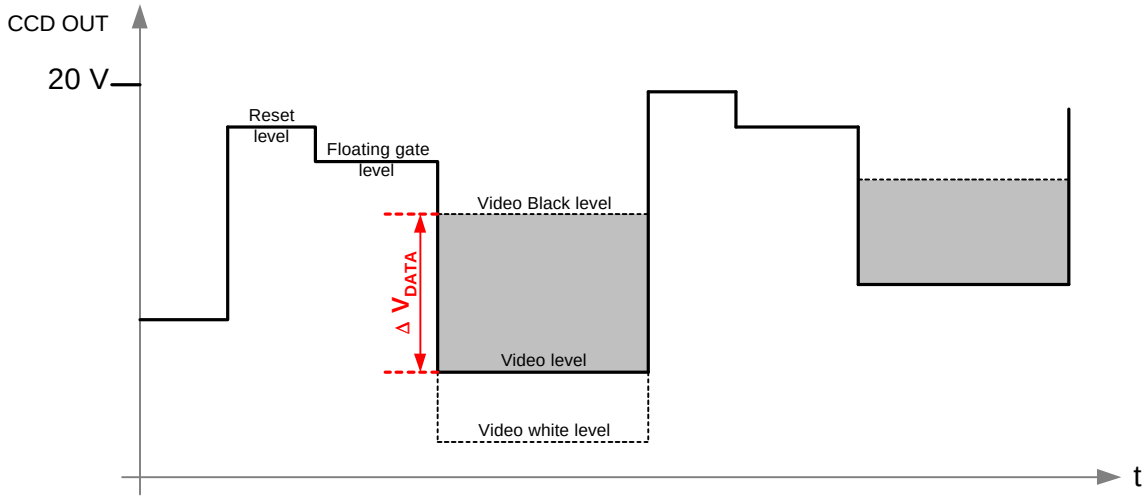

Figure 2. CCD video signal

- First the sensing capacitor charge is initialized to supply voltage (20V typ.) through the R_{on} of the output MOS switch. It results in a reset peak often called *reset feedthrough level.*

- Then, when the switch is opening, the switch parasitic capacitor is put in parallel with the sensing capacitor, hence the reset voltage across those capacitors decreases to a level called *floating gate level*.
- At last, the sensing capacitor collects the electrical charges resulting from light integration. This is the active video.

3 INPUT BUFFER

The useful output data is the difference between the Black level and the Video level. It will be obtained thanks to the CDS stage which will store the analog levels Black and Video in two internal capacitors that are located at the device input.
Many competitors advise to use an external output buffer to drive those capacitors but taking care of the current needed (3 mA and more) and of the power supply (more than 15 V), you have to take into account more than 45 mW extra power consumption.
Thanks to its internal input buffer, TDA9952 doesn't need an additional external buffer in most of cases. If the output of the CCD is high impedance -depending on the CCD type and on the connection length between CCD and the CDS input, only a very small external buffer will be needed.

4 INPUT CLAMP (CLPDM)

The common-mode level of the image sensor's output signal could range from 0 V to more than 10 V, so the signal must be ac-coupled the TDA9952.

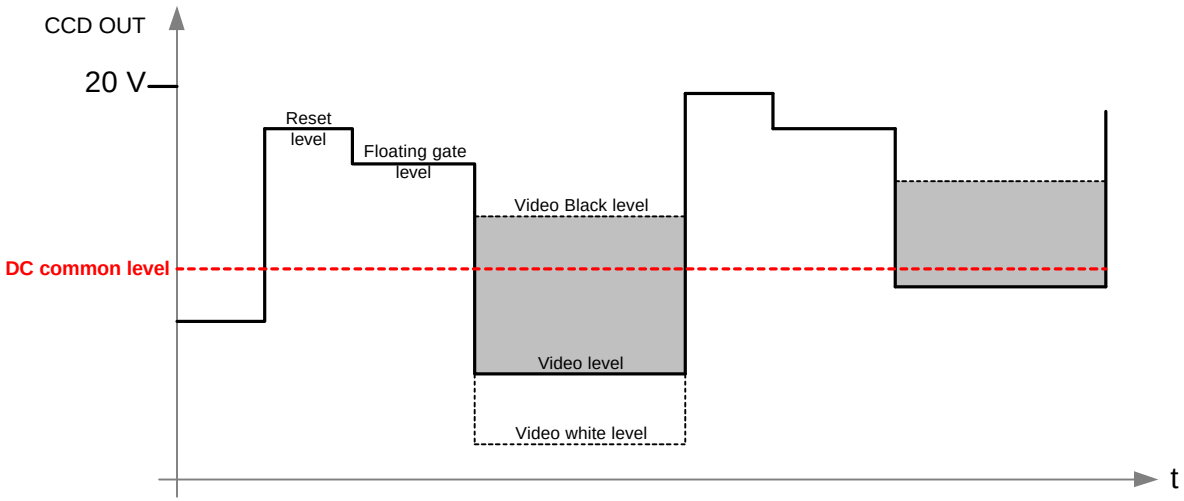

Figure 3. DC common-mode level of a CCD video signal

The input clamp restores the dc level of the signal to an optimum point within the supply range of the device thanks to a serial capacitor. This one shifts the floating gate level to the internal reference level V_{CLPDM}, around 1.7 V.
According to formula $V_{CLPDM} = V_{CC} - 0.7V - V_{BE}$, this reference depends on power supply voltage and operating temperature (example : at 25° and V_{CC}=3.3V then $V_{CLPDM} \approx 1.8V$).

The input clamp can be used in many ways.

- We can set the clamp active on the dummy pixels. Then we need a big capacitor to keep a stable V_{CLPDM} on all the line.
- We can set the clamp active on all the line. Then we need a small capacitor because we refresh it every pixel. Depending on the application, a small additional noise could be seen at the output.
- But we can't set CLPDM and CLPOB (optical black clamp loop, see Chapter 6) active at the same time during the black pixels.

To choose the good value for the serial input capacitor, we have to take care of two parameters.

- A current of few µA is leaking from the input pin IN. That is why the capacitor's value needs to be high enough in order to avoid an offset and then preserve the dynamic range of the incoming video signal.
- To ensure a good start-up time, a too big capacitor should be avoided.

5 CORRELATED DOUBLE SAMPLER

The principle of Correlated Double Sampling (CDS) is to measure twice in a pixel period the signal level coming out of the CCD. Data is obtained by removing the video data level (sampled by SHD) and the offset between the floating gate level and the black level (see Chapter 6) from the floating gate level (sampled by SHP).. This process is depicted in Figure 5.

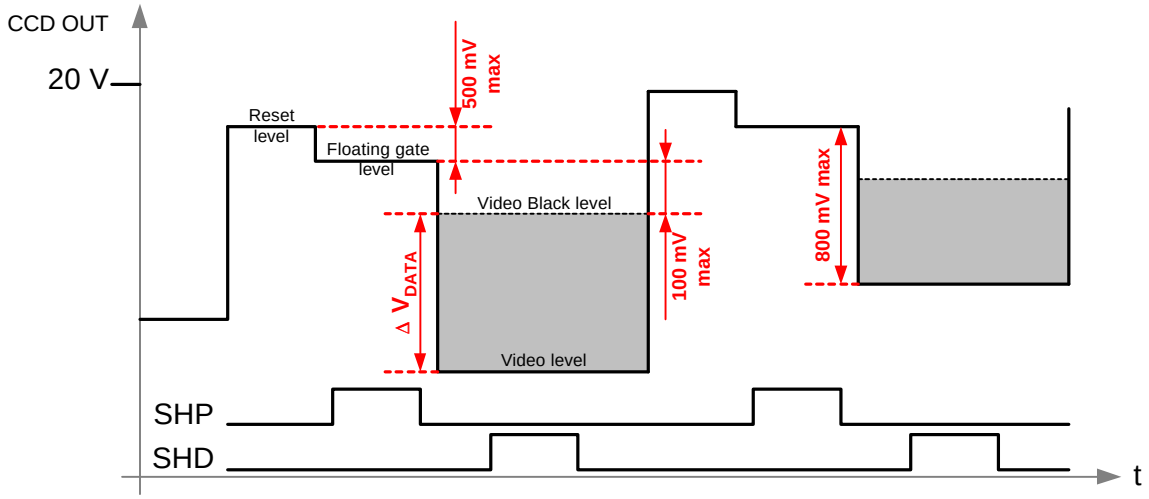

Figure 4. CCD signal sampling and limiting values

Sampling of floating gate and video levels should be adjusted to reach the best performances.

- The sampling pulses width should be as large as possible to reach the highest step transitions.
- Timing th1 and th2 must be respected. Those timings are due to the different processing delays of the CCD signal, the SHP and SHD signals inside the chip.

Main parameters concerning the voltage applied to pin IN have the following limiting values.

- The reset level should never exceed 500 mV.
- The maximum black offset is 100mV.
- The maximum input signal (Floating gate level – Video level) is 800 mV at 3 V.

The reset switch generates noise which results in a shift of the reset reference level, as described in Figure 5.

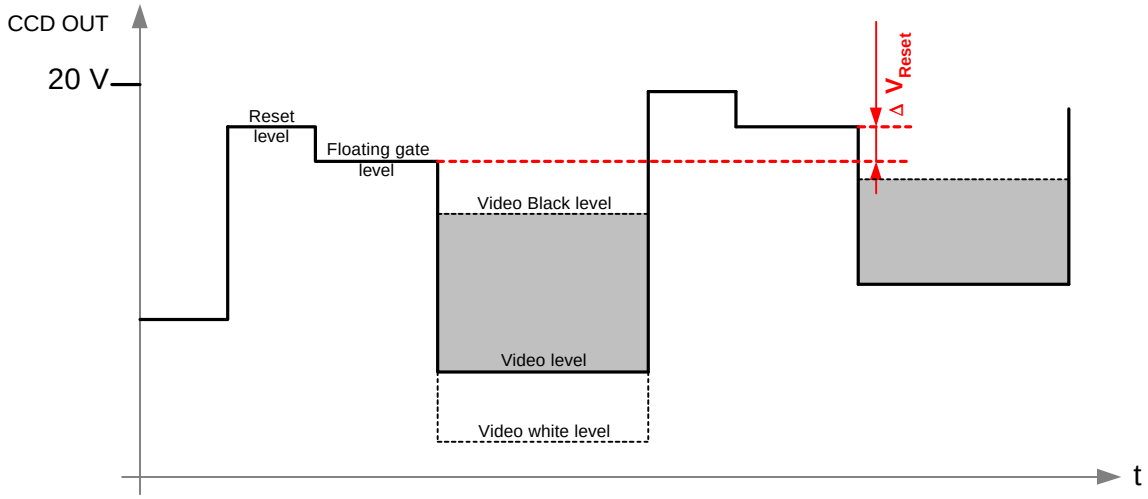

Figure 5. Reset noise effect on two consecutive pixels

This shift affects similarly the floating gate level and the video level but it differs from one pixel to the other. The reset noise of the CCD output buffer is correlated between SHP and SHD samples, that is why the CDS will remove the offset and also every low frequency noise compared to pixel frequency.

6 OPTICAL BLACK CLAMP LOOP (CLPOB)

Usually the video level coming out of the CCD is not equal to the floating gate level even if no light has been collected by the pixel. Dark current and clock feedthrough noise cause this shift called ΔV_{Black} between floating gate level and what is called black level.

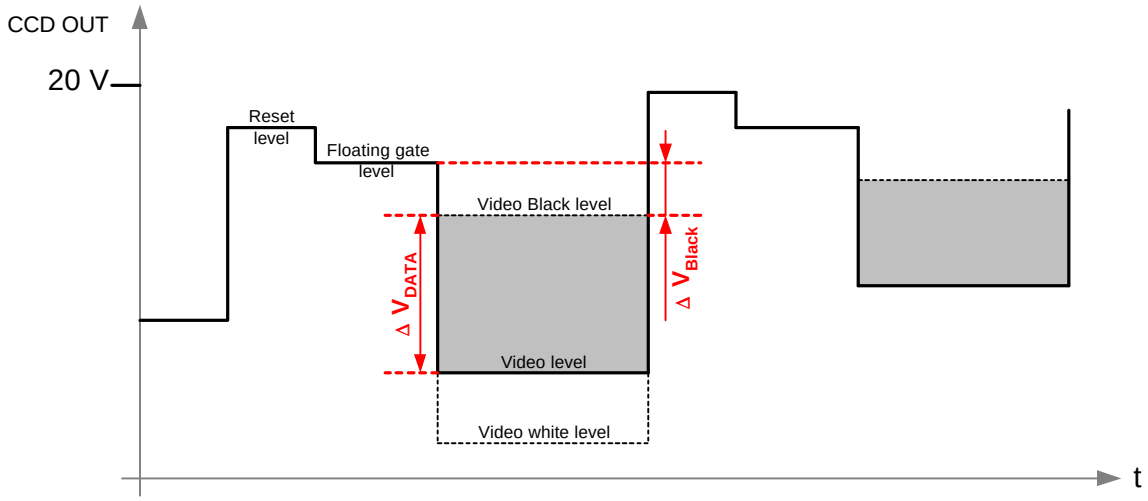

Figure 6. Black Offset and Data

This offset shouldn't be taken into account in video level to know which is the amount of light the pixel has collected. That is why it must be removed before amplification to preserve the video dynamic range, especially in low light conditions when ΔV_{DATA} could become smaller than ΔV_{Black}.

To remove the ΔV_{Black} level from the video signal, an optical black clamp loop circuitry is implemented inside the preprocessor. Through the pixel stream coming out of the CCD, some pixels called "optical black pixels" are used as reference to measure ΔV_{Black}. The CLPOB signal indicates to the preprocessor that ΔV_{Black} calibration has to be done.

Depending on the application targeted, the capacitors associated with black clamp calibration (CPCDS1 and CPCDS2) must be adjusted.

- To decrease clamp noise by a factor n, one can multiply by n^2 the clamp capacitor value.
- The charge current depends on the gain when the established value is approached (8 times more current at minimum gain than at maximum gain). So the clamp capacitors must be big enough to avoid oscillations at minimum gain.
- Increasing the clamp capacitor value also increases the start up time of the system.

If one needs a small capacitor value on the clamp capacitors CPCDS1 and CPCDS2 in order to improve start-up time but if oscillations on capacitors are feared, the minimum charge current can be set.
Considering Io as the defect maximum current value at initialization and the following table as the serial interface programming, it will give:

Address bits A3 to A0					Data bits SD11 to SD0												Maximum current
3	2	1	0		11	10	9	8	7	6	5	4	3	2	1	0	
0	1	0	0		X	X	X	X	0*	1*	1*	1*	1*	0	0	0	1 x (Io/8)
														0	0	1	2 x (Io/8)
														0	1	0	3 x (Io/8)
														:	:	:	:
														1	1	1	8 x (Io/8)

X stands for “non-used bit”
* stands for “must be set to the indicated value”
Then it is possible to boost the current at the beginning and reduce it via the serial interface when the clamp balance is near.

So the timing diagram and the signals’ waveforms will be the following:

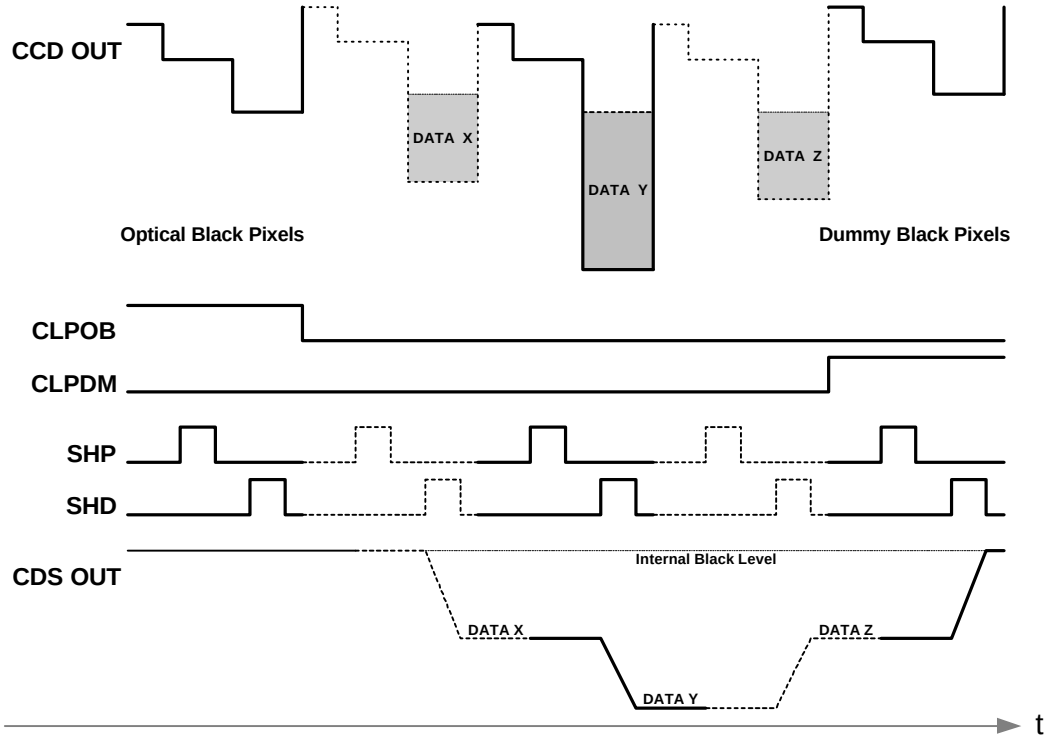

Figure 7. Timing diagram

7 PROGRAMMABLE GAIN AMPLIFIER

The goal of PGA is to amplify the differential voltage obtained thanks to the CDS to use the maximum input range of the ADC. The PGA gain is programmable from -2.5 dB to 33.5 dB via the 3 wires serial interface. Taking into account the gain of the other blocks, full scale output (code 0 to 1023 at ADC output) will be reached with an input amplitude ΔV_{DATA} of 800mV and the gain code setting 0.

The equation of gain, described on Figure 8, is the following.

- For code between 0 and 383 : $Gain_{dB} = \left(\frac{Code}{383} * 36dB \right) - 2.5dB$
- For code between 383 and 511, gain is set to 33.5dB

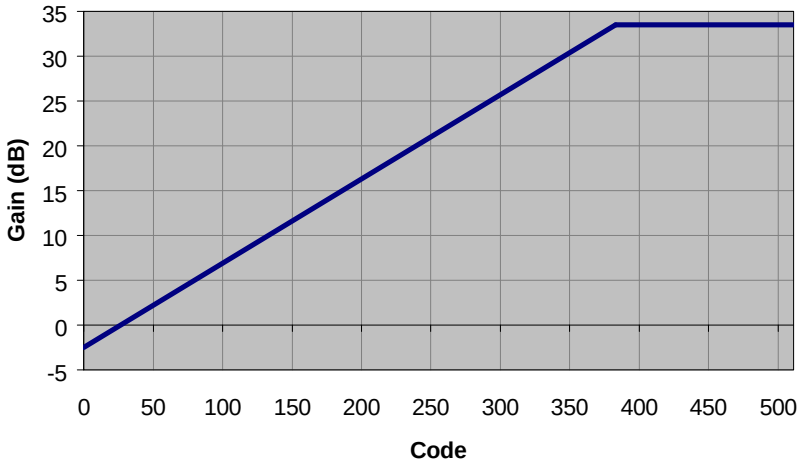

Figure 8. PGA Gain = f(Code)

The main characteristics of PGA are:

- Setting over 9 bits
- Gain range = 36dB
- Steps = 0.1dB +/- 0.02 dB
- Integral Non Linearity(max) = +/- 0.033dB

When the maximum ΔV_{DATA} value in mV (DataMax) on a frame is known, the code to be set in order to have a full scale input is given by the following equation:

$$Code = \frac{20 \cdot \log\left(\frac{800mV}{DataMax} \right)}{36dB} \cdot 383$$

8 CONTROL INPUTS

An extra information about the control inputs is useful in order to set the device in the best state during start-up and stand-by time.

STDBY pin is used to put the device in waiting state for being started quickly. The serial interface is still active in stand-by mode and the digital output pins will be set at the programmed clamp code.

BLK pin is used to determine the active window where the processing has to be done. Outside this window, the digital output will be set at the programmed clamp code.

VSYNC signal is used with SEN signal to activate in the device the settings programmed via the serial interface. Settings will be active only after a rising edge in a first time of SEN and an active edge of VSYNC in a second time. To be able to change settings in a frame, you just need to connect SEN and VSYNC together.

To choose the active edge or level of VSYNC, BLK, STDBY and all the other control inputs, see "table 2: Polarity settings", page 17 in the specification. When power supplies increase from zero, the settings programmed by defect are:

- Polarity settings:

Address bits A3 to A0					Data bits SD11 to SD0												Comment
3	2	1	0		11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	1		X	X	0	1	1	1	1	1	1	1	1	1	All the control pulses are active on rising edge or high level.

- PGA gain code is set to 000
- Clamp code is set to 00
- Input OFD is set to logic 0

9 LAYOUT AND IMPLEMENTATION INFORMATION

The TDA9952 is a high speed and high precision analog circuitry combined with an analog to digital converter. To get the most of its performances this IC has to be treated as an analog component and should be properly decoupled from wideband noise generated by digital circuitry.

The following diagram is shown to identify most critical pins. Power supply pins must be carefully decoupled with 0.1µF ceramic chip capacitors close to the IC. Short leads length and low ground impedance are important to reach the best performance.

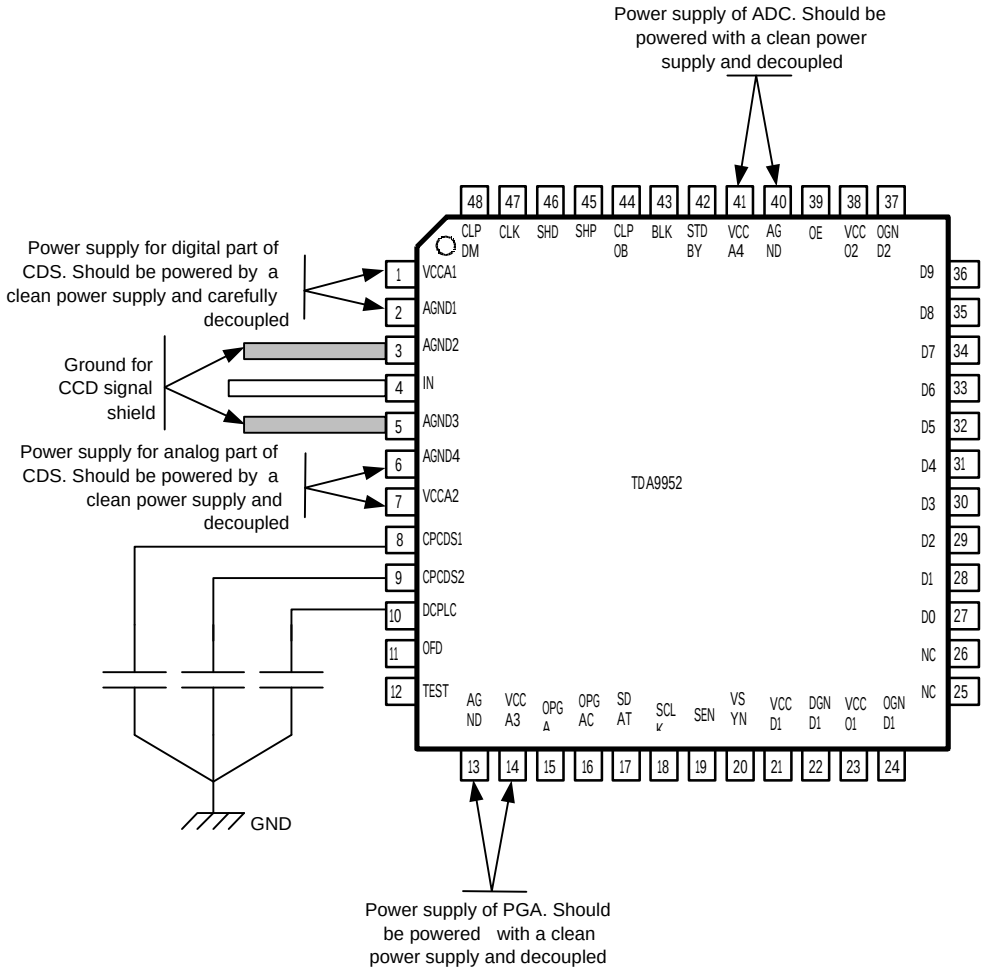

Figure 9. Advice about main sensitive pins

It is recommended to protect the input signal with a shield made of a clean ground which will be connected to input pins 3 and 5.

It is important that pins 8, 9 and 10 have ground potentials as close as possible to each other. This can be achieved by connecting traces to the ground plane at the same point on the layout. Following this advice helps to improve noise performance.

Special care has to be taken when driving inputs with high-speed digital ICs. Due to their very high slew rate, high-speed digital circuits generate high frequencies. Those, due to bad impedance matching, are able to generate overshoots and undershoots beyond power supply potentials. In general adding resistors in series with digital signals will remove offending transients and prevent them from disturbing internal circuitry.

The digital lines that this IC will have to drive towards the DSP may be highly capacitive. In this case high intensity instantaneous current will flow through output buffers to charge the parasitic capacitance. Those currents could feed back into the analog region and affect the performances of the circuit. Either using damping resistors or buffers in series with each data line may help to reduce the surge current.

The next figures will show the implementation made by Philips for the evaluation of the device in a HVQFN package:

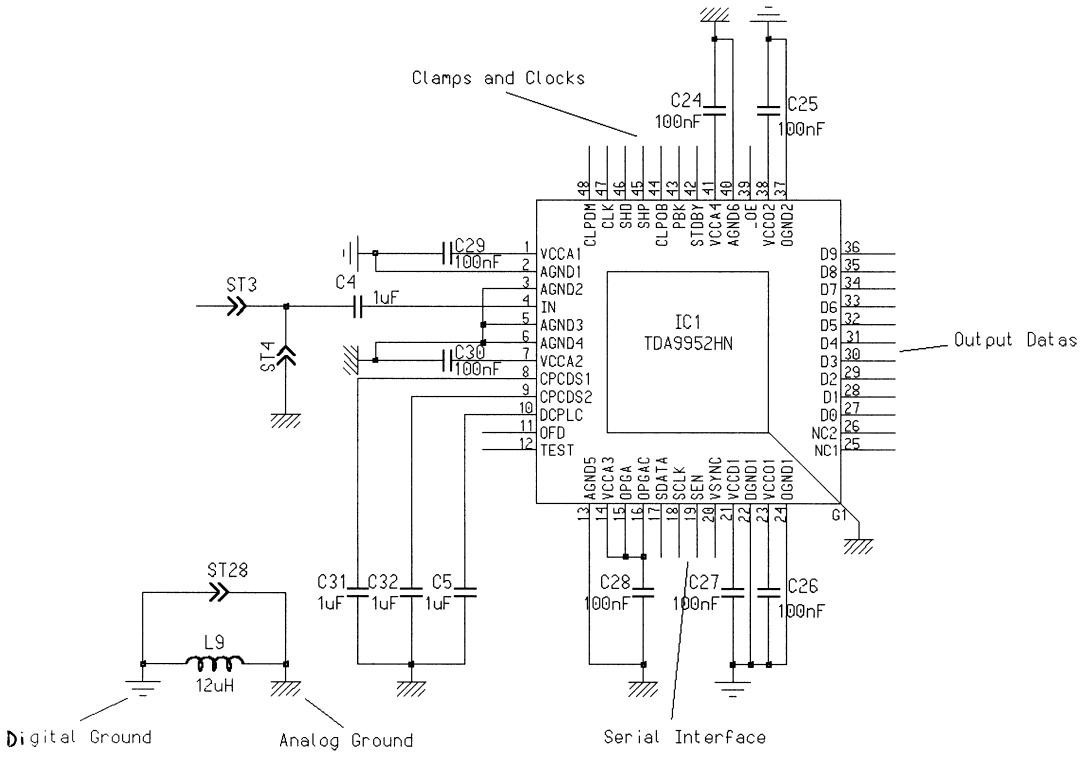

Figure 10. Electrical schematic

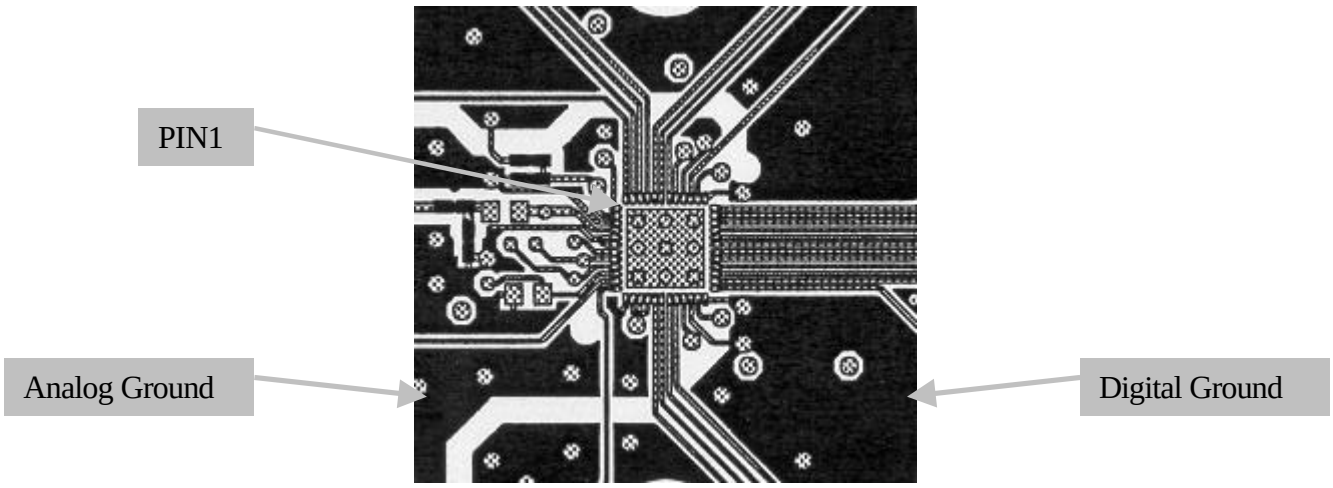

Figure 11. Top layer design

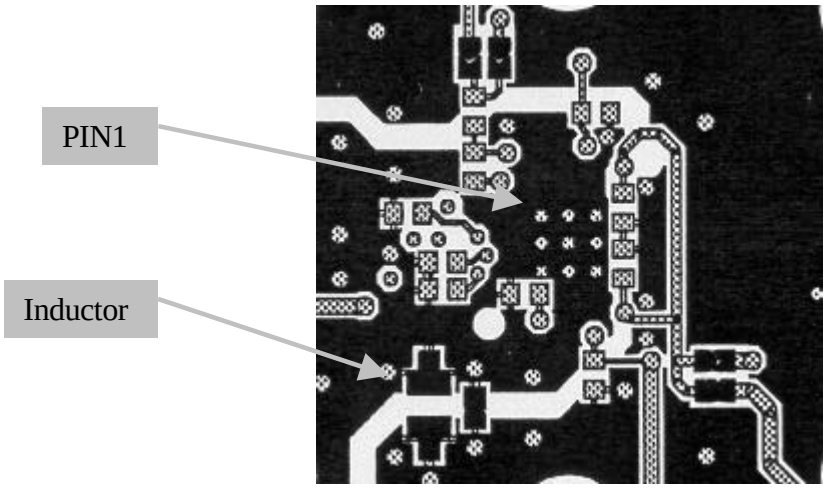

Figure 12. Bottom layer design

If possible we advise to separate analog and digital ground and to connect them with an inductor in order them to have the same dc voltage. In this case, connect the expose die pad to the analog ground in several points.

10 APPLICATION DIAGRAM

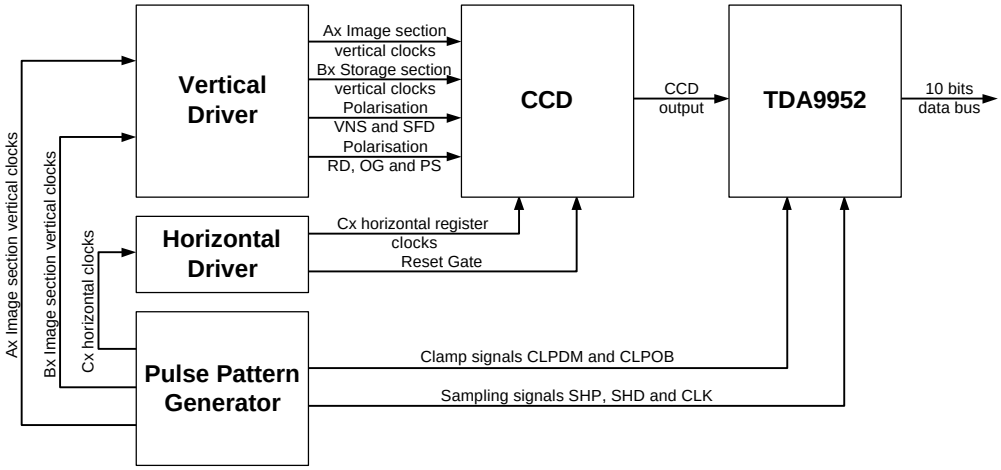

Figure 13. Imaging chipset example

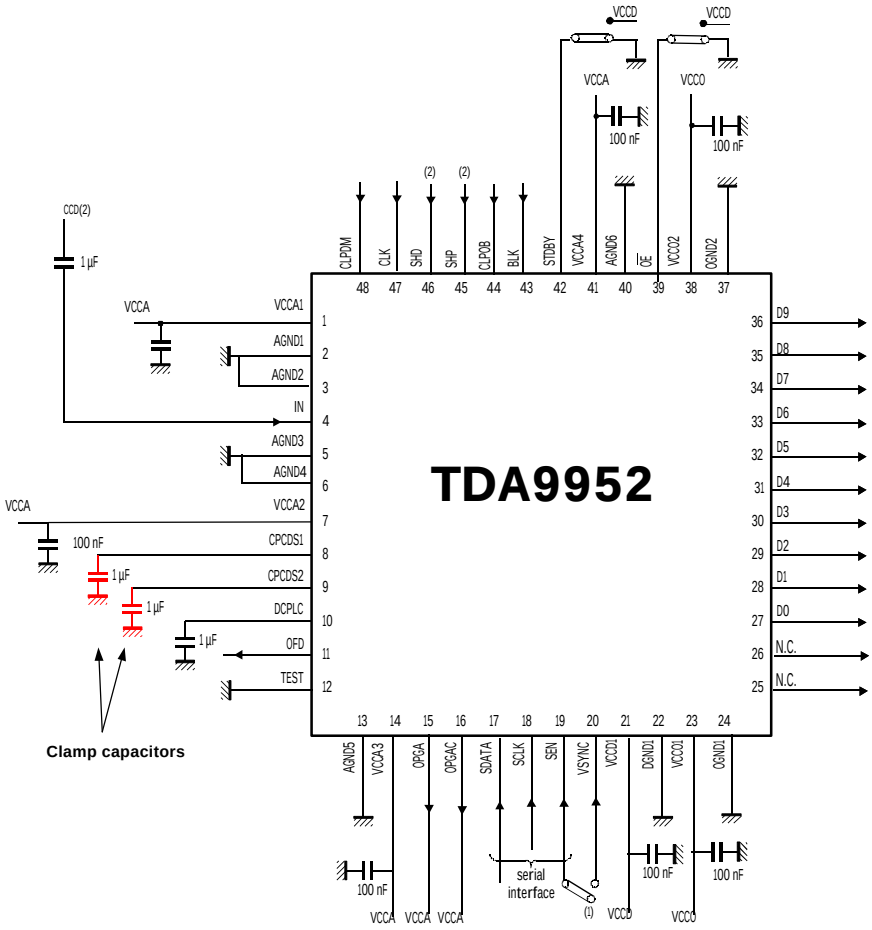

Figure 14. TDA9952 application diagram

11 LIST OF FIGURES

GLOSSARY

AC Alternative Current
ADC Analog to Digital Converter
CCD Charge Coupled Device
CDS Correlated Double Sampling
DC Direct Current / Continuous level
PGA Programmable Gain Amplifier
DN Digital Number